WHAT WE CLAIMED ARE:

1. A semiconductor device, which comprises a capacitor comprising a lower electrode layer, a ferroelectric layer and an upper electrode layer, wherein a convex or concave region is formed on the upper surface of the ferroelectric layer.

2. The semiconductor device according to claim 1, wherein the convex or concave region formed on the upper surface of the ferroelectric layer is thoroughly covered with the upper electrode layer.

3. The semiconductor device according to claim 1, wherein a convex or concave region is formed also on the upper surface of the lower electrode layer.

4. The semiconductor device according to claim 3, wherein the convex or concave region formed on the upper surface of the ferroelectric layer is thoroughly covered with the upper electric layer, and the convex or concave region formed on the upper surface of the lower electrode layer is thoroughly covered with the ferroelectric layer.

5. The semiconductor device according to claim 1 or 2, wherein a height or a depth of the convex or concave region formed on the upper surface of the ferroelectric layer is half or smaller than the thickness of the ferroelectric layer, and is in a range from the same as to half the thickness of the upper electrode layer.

6. The semiconductor device according to claim 1 or 2,

wherein a height or a depth of the convex or concave region formed on the upper surface of the ferroelectric layer is half or smaller than the thickness of the ferroelectric layer, and is in a range from the same as to half the thickness of the upper electrode layer, and a height or a depth of the convex or concave region formed on the upper surface of the lower electrode layer is half or smaller than the thickness of the lower electrode layer, and is in a range from the same as to half the thickness of the ferroelectric layer.

7. A process for manufacturing a semiconductor device which has a capacitor comprising a lower electrode layer, a ferroelectric layer and an upper electrode layer, which comprises a step of forming a convex or concave region on the upper surface of the ferroelectric layer so that the upper electrode layer thoroughly covers the convex or concave region formed on the upper surface of the ferroelectric layer.

8. The process for manufacturing a semiconductor device according to claim 7, which further comprises a step of forming a convex or concave region also on the upper surface of the lower electrode layer so that the ferroelectric layer thoroughly covers the convex or concave region formed on the upper surface of the lower electrode layer.